REMARKS

In response to the Office Action dated 2/28/2007, please consider the following discussion.

Claims 1, 4, 5, and 8 remain in the case. No new claims are added and none canceled by this response.

The remaining claims are rejected in the Office Action under 35 U.S.C. 103(a) as unpatentable over Shim et al. (US 6,531,784) in view of Kang et al. (US 2003/017810 A1).

Claim 1 (Claim 5 has a similar limitation) has the following limitation:

electrical conductive runs on the substrate that run substantially under the die connecting the first substrate contacts, wherein the first substrate contacts are located adjacent to the first side of the die, to second substrate contacts,

This limitation of running under the die provides the advantage of allowing a die-up die to be packaged in a die-down package. It provides the side to side reversal of the contacts so that the die contacts match those of the package regardless of the "die-up" or "die-down" types.

The Office Action at the top of page 3 states that,

"substrate contacts 22" and continues with:

"...electrical conductive runs 24 on the substrate that run substantially under the die connecting the first substrate contacts, wherein the first substrate contacts are located

adjacent to the first side of the die, to second substrate contacts 22, wherein the second substrate contacts are located adjacent to the opposite side of the die..." (underlining added).

I do not understand the Examiners conclusion, please the above phrase is not shown, discussed or supported anywhere in the Shim reference, and Kang does not help.

First, quoting from Shim's column 3, lines 46 et seq., layers 22 and 24 are:

"...conductive layers 22, 24 of a metal...that comprise the top and bottom surfaces of the substrate, respectively. The conductive layers 22, 24 are typically patterned, e.g., by photolithography techniques, to define terminal pads 26 in the top layer 22 and solder ball lands 28 in the bottom layer 24."

The references 22 and 24 refer to layers, not conductive runs in the metal layers 22 and 24.

FIGs. 1-3 show conductive runs, the pads 26, vias 30, and the vias 30 connecting to pads 28 that are connected to solder balls 18. None of the conductive runs from pads 26 to vias 30 run under the IC 14, and there are no runs shown in the bottom layer 24. Also, there is no discussion of runs under the IC's 14 and 16. Note that all the contacts on the ICs 14 and 16 are connected to pads 26 and conductive runs.

That brings us to FIGs. 7, 8 and 9. These FIGs. show additional solder balls that protrude through the solder mask layer 32 and contact the metal layer 24, but no connection to vias are shown. Solder balls labeled 18 make electrical connections to the ICs 14 and 16 as shown in FIGs. 2, 2A and 3, but there is no label or discussion of the middle unreferenced solder balls. Also, in FIGs. 7-9, there are unreferenced vias under the die 14, but notice that there are no possible connections from IC's 14 and 16 to the top metal

layer 22 under the ICs that might connect to the unreferenced vias. The layer 22 under the ICs is interrupted in all the FIGs. and the IC contacts cannot connect to a run that then connects to the top of the unmarked vias in layer 22 under the ICs. FIGs. 1, 2, 2A and 3, show all the contacts on the IC's 14 and 16 connected to runs and none travel under the chip, and there is nothing to suggest a need to travel under the ICs, and it is impossible to make such connections with the interruption of layer 22 under the ICs.

The Examiner states that "..electrical conductive runs 24 on the substrate that run substantially under the die..", but such is not shown or discussed. The Examiner must be assuming something not shown.

The best explanation for these unreferenced balls is shown in FIG. 11. The IC is square with contacts around the entire periphery and from any angle there will be solder balls across the horizontal view.

In summary, there are no conductive runs shown under the IC chips, there is no such discussion, and there is no advantage or need mentioned in the cited references to suggest making runs under the chips.

I left a telephone message with the Examiner asking that he call me. I would appreciate the Examiner fully evaluating the above, and calling me if there is some misunderstanding on my part. This application has had a very long prosecution, and I would appreciate the Examiner conferring with a colleague on this response.

Please charge any additional fee occasioned by this paper to our Deposit Account No. 03-1237.

Respectfully submitted,

/Edwin H. Paul/

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